(3) Japanese Patent Application Laid-Open No.11-238734 (1999):
"SEMICONDUCTOR INTEGRATE CIRCUIT"

The following is a brief description of the invention disclosed in this publication.

Figure 1 is a cross section showing the configuration of the semiconductor integrated circuit in the first embodiment of the invention. In Fig. 1, 1 shows a transistor of N channel, 1D shows a drain of the transistor 1, 1G shows a gate of the transistor 1, and 1S shows a source of the transistor 1. 2 shows a wiring, to which the attention is paid, provided in a fifth layer (a top layer), 3 shows wirings in the first layer to the fourth layer which provide a signal from the transistor 1 to the wiring 2, 4A, 4B,... are gates which input a signal from the wiring 2, and 6A, 6B,... are wirings which branch a signal into the gates 4A and 4B from the wiring 2, which is five layers above. 5 is a heat dissipation wiring prepared for heat dissipation in P-type silicon substrate 9 which is located in the lowest layer directly under from the wiring 2.

The heat dissipation wiring 5 is comprised of a contact 5A, a first layer wiring 5B, a first-to-second-layer through hole 5C, a second layer wiring 5D, a second-to-third-layer through hole 5E, a third layer wiring 5F, a third-to-fourth-layer through hole 5G, a fourth layer wiring 5H, and a fourth-to-fifth-layer through hole 5I, which can be formed in the same manufacturing process as other wirings. Therefore, the increase of the manufacturing process to form the heat dissipation wiring 5 can be avoided, and a rise of the manufacturing cost will be hold down.

In a surface of the P-type silicon substrate 9 where the transistor 1 is not formed a thick field oxide film 8 called LOCOS (Local Oxidation of Silicon) is provided. The field oxide film 8 is not provided in a contact portion 7 where the contact 5A on the P-type silicon substrate 9 is contacted (connected), thus, P-type silicon substrate 9 is exposed as it is.